The Following Is Claimed:

1. A digital cross connect system, comprising:

a switch matrix subsystem comprising a plurality of switch matrix units in a CLOS arrangement in multiple stages, each switch matrix unit having a plurality of input ports and output ports, at least two of the switch matrix units having a number of their output ports uniquely connected to input ports on one of the switch matrix units in the next stage and having an equal number of their output ports uniquely connected to input ports on another of the switch matrix units in the next stage;

a plurality of subsystem input ports associated with the switch matrix subsystem;

a plurality of subsystem output ports associated with the switch matrix subsystem; and

switch matrix unit programming that instructs the switch matrix units to generate specific internal cross-connections that allow one or more input signals present at one or more subsystem input ports to be connected to one or more subsystem output ports.

2. The system of claim 1 wherein the switch matrix subsystem comprises a three-stage architecture having at least two switch matrix units in each stage.

3. The system of claim 2 wherein the inputs ports of the first stage switch matrix units are inputs ports for the switch matrix subsystem and the output ports of the third stage switch matrix units are output ports for the switch matrix subsystem, each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit, each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage.

4. The system of claim 1 wherein the switch matrix unit programming is generated by a method with steps comprising:

obtaining information that identifies a specific subsystem input port and a desired subsystem output port for connecting to the specific subsystem input port;

identifying a pathway from a switch matrix unit in the cross connect system that provides the specific subsystem input port to a switch matrix unit in the cross connect system that provides the desired subsystem output port;

determining that sufficient channels exist in the identified pathway to allow a connection from the specific subsystem input port to the desired subsystem output port;

identifying specific channels in the identified pathway to allow a connection from the specific subsystem input port to the desired subsystem output port; and

storing in a programming data structure information identifying connections that have to be made in a plurality of switch matrix units in the cross connect system to allow the connection from the specific subsystem input port to the desired subsystem output port.

5. The system of claim 1 wherein the programming comprises instructions stored in memory.

6. The system of claim 1 wherein the programming comprises an arrangement of binary values stored in memory.

7. The system of claim 1 wherein the programming comprises software code stored in memory.

8. The system of claim 5 or 6 wherein the memory comprises Read Only Memory.

9. The system of claim 5 or 6 wherein the memory comprises Random Access Memory.

10. The system of claim 1 wherein the programming comprises a programmable circuit element that have been programmed.

11. The system of claim 10 wherein the programmable circuit element comprises an application specific integrated circuit.

12. The system of claim 10 wherein the programmable circuit element comprises a programmable logic array.

13. The system of claim 1 wherein each switch matrix unit comprises an application specific integrated circuit.

14. The system of claim 1 wherein each switch matrix unit comprises a square matrix.

15. The system of claim 1 wherein the number of input ports for each switch matrix unit is the same.

16. An apparatus that performs a switching function, comprising:

a plurality of switch matrix units each having input ports and output ports, at least six of said switch matrix units are organized in three stages with two switch matrix units in each stage, the inputs ports of the first stage switch matrix units being inputs ports for the apparatus and the output ports of the third stage switch matrix units being output ports for the apparatus, each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit, each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage; each switch matrix unit being programmable to provide connections between its input ports and its output ports; and

switch matrix unit programming for each first stage, second stage and third stage switch matrix units, the programming instructing at least one of the first stage switch matrix units, at least one of the second stage switch matrix units and at least one of the third stage switch matrix units to each establish an internal connection that allows a signal appearing at one of the inputs of the apparatus to be switched to at least one of the outputs of the apparatus.

17. The apparatus of claim 16 wherein the programming is generated using a method with steps comprising:

obtaining information that identifies an input port of the apparatus and a desired output port of the apparatus for connecting to the identified input port;

identifying a pathway from a switch matrix unit in the apparatus that provides the identified input port to a switch matrix unit in the apparatus that provides the desired output port;

determining that sufficient channels exist in the identified pathway to allow a connection from the identified input port to the desired output port;

identifying specific channels in the identified pathway to allow a connection from the identified input port to the desired output port; and

storing in a programming data structure information identifying connections that have to be made in a plurality of switch matrix units in the apparatus to allow the connection from the identified input port to the desired output port.

18. A method for generating switch matrix unit programming for switch matrix units of a cross connect device, comprising:

obtaining information that identifies an input port of the cross connect device and a desired output port of the cross connect device for connecting to the identified input port;

identifying a pathway from a switch matrix unit in the cross connect device that provides the identified input port to a switch matrix unit in the cross connect device that provides the desired output port;

determining that sufficient channels exist in the identified pathway to allow a connection from the identified input port to the desired output port;

identifying specific channels in the identified pathway to allow a connection from the identified input port to the desired output port; and

storing in a programming data structure information identifying connections that have to be made in a plurality of switch matrix units in the cross connect device to allow the connection from the identified input port to the desired output port.

19. The method of claim 18 further comprising using the programming data structure to generate the switch matrix unit programming for switch matrix units of the cross connect device, the switch matrix unit programming identifying internal connections that have to be made within the switch matrix units to connect the identified input to the desired output.

20. The method of claim 18 wherein the step of identifying a pathway comprises identifying a preferred pathway instead of an alternate pathway.

21. The method of claim 20 wherein the step of identifying a preferred pathway comprises identifying the preferred pathway when the alternate pathway was identified in a prior iteration.

22. The method of claim 18 wherein the step of identifying a pathway comprises identifying an alternate pathway instead of a preferred pathway.

23. The method of claim 22 wherein the step of identifying an alternate pathway comprises identifying the alternate pathway when the preferred pathway was identified in a prior iteration.

24. The method of claim 18 wherein the step of determining that sufficient channels exist comprises:

remembering the number of available output ports for a plurality of the switch matrix units; and

determining that each switch matrix unit that has output ports in the identified pathway has an available output port.

25. The method of claim 24 wherein the remembering step comprises keeping a count of the number of output ports that are not available.

26. The method of claim 25 wherein the step of identifying specific channels comprises incrementing the count of output ports that are not available.

27. The method of claim 18 wherein the step of identifying specific channels comprises:

identifying specific output ports in specific switch matrix units that are in the identified pathway that are available; and

reserving the identified specific output ports for use in making the connection from the identified input port to the desired output port.

28. The method of claim 27 wherein the step of identifying specific output ports comprises:

assigning a numerical value to the output ports; and

identifying available output ports that have the lowest numerical value.

29. The method of claim 18 wherein the step of obtaining information that identifies an input port comprises obtaining information that identifies a plurality of input port and desired output port pairs.

30. The method of claim 29 wherein the input port and desired output port pairs are grouped such that all pairs having the same entry switch matrix unit and exit switch matrix unit are grouped together.

31. The method of claim 30 wherein the plurality of input port and desired output port pairs includes at least one input port that is to be connected to more than one output port.

32. The method of claim 31 wherein the input ports having the same entry switch matrix unit and multiple exit switch matrix units are grouped together.

33. The method of claim 32 wherein the steps of claim 8 are repeated for all of the input port and desired output port pairs.

34. The method of claim 33 wherein the input ports that are to be connected to more than one output port are selected for processing before the groups of input port and desired output port pairs having the same entry switch matrix unit and exit switch matrix unit.

35. A method for programming an apparatus having at least six switch matrix units wherein the six switch matrix units are organized in three stages with two switch matrix units in each stage, the inputs ports of the first stage switch matrix units being inputs ports for the apparatus and the output ports of the third stage switch matrix units being output ports for the apparatus, each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit, each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage, each switch matrix unit being programmable to provide connections between its input ports and its output ports, the method comprising:

calculating a path for a signal on an input port for the apparatus to an output port for the apparatus; and

programming at least one of the first stage switch matrix units, at least one of the second stage switch matrix units and at least one of the third stage switch matrix units to each establish an internal connection that allows a signal appearing at the input port for the apparatus to be connected to an output port for the apparatus.

36. The method of claim 35 wherein the calculating step comprises

identifying a pathway from a switch matrix unit in the apparatus that provides the input port to the switch matrix unit in the apparatus that provides the desired output port;

determining that sufficient channels exist in the identified pathway to allow a connection from the identified input port to the desired output port; and

identifying specific channels in the identified pathway to allow a connection from the identified input port to the desired output port.